Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (original) A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to tie bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction specifying both a shift amount and a register having a register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width, the execution unit is operable to:

(i) shift a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and

(ii) provide the second plurality of data elements as a catenated result.

2. (original) The system of claim 1 wherein the catenated result is provided to a register.

3. (original) The system of claim 1 wherein the shift amount is contained in a register specified by the instruction.

4. (original) The system of claim 1 wherein the shift amount is contained in an immediate field of the instruction.

5. (original) The system of claim 1 wherein each data element in the first plurality of data elements has a sign bit in a most significant bit position and wherein the execution unit is further operable to fill a shift amount number of most significant bit; in each of the second plurality of data elements with the sign bit from a respective data element in the first plurality of data elements.

6. (original) The system of claim 1 wherein the execution unit is further operable to fill a shift amount number of most significant bits in each of the second plurality of data elements with zeros.

7. (original) The system of claim 1 wherein the execution unit is further operable to fill a shift amount number of most significant bits in each of the second plurality of data elements with a subfield from a respective location of the contents of an additional register.

8. (original) The system of claim 1 wherein the catenated result has a width of 128 bits.

9. (original) The system of claim 1 wherein the elemental width of each of the first plurality of data elements is 32 bits.

10. (original) The system of claim 1 wherein the elemental width of each of the first plurality of data elements is 16 bits.

11. (original) The system of claim 1 wherein an elemental width of each of the second plurality of data elements is equal to the elemental width of each of the first plurality of data elements.

12. (original) The system of claim 1 wherein an elemental width of each of the second plurality of data elements is equal to twice the elemental width of each of the first plurality of data elements.

13. (original) The system of claim 1 wherein an elemental width of each of the second plurality of data elements is equal to half the elemental width, of each of the first plurality of data elements.

14. (currently amended) A computer-readable storage medium:

having instructions that cause a computer system to perform operations,

wherein at least some of the instructions comprise a group shift instruction for shifting data in a programmable processor, the group shift instruction:

specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift amount configurable to an amount inclusively between :zero and one less than the elemental width;

shifting a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and

providing the second plurality of data elements as a catenated result.

15. (currently amended) The computer-readable storage medium of claim 14 wherein the catenated result is provided to a register.

16. (currently amended) The computer-readable storage medium of claim 14 wherein the shift amount is contained in a register specified by the instruction.

17. (currently amended) The computer-readable storage medium of claim 14 wherein the shift amount is contained in an immediate field of the instruction.

18. (currently amended) The computer-readable storage medium of claim 14 wherein each data element in the first plurality of data elements has a sign bit in a most significant bit position and wherein the group shift instruction further comprises:

filling a shift amount number of most significant bits in each of the second plurality of data elements with the sign bit from a respective data element in the first plurality of data elements.

19. (currently amended) The computer-readable storage medium of claim 14 wherein the group shift instruction further comprises: filling a shift amount number of bits in each of the second plurality of data elements with zeros.

20. (currently amended) The computer-readable storage medium of claim 14 wherein the group shift instruction further comprises: filling a shift amount number of bits in each of the second plurality of data elements with a subfield from a respective location of the contents of an additional register.

21. (currently amended) The computer-readable storage medium of claim 14 wherein the catenated result has a width of 128 bits.

22. (currently amended) The computer-readable storage medium of claim 14 wherein the elemental width of each of the first plurality of data elements is 32 bits.

23. (currently amended) The computer-readable storage medium of claim 14 wherein the elemental width of each of the first plurality of data elements is 16 bits.

24. (currently amended) The computer-readable storage medium of claim 14 wherein an elemental width of each of the second plurality of data elements is equal to the elemental width of each of the first plurality of data elements.

25. (currently amended) The computer-readable storage medium of claim 14 wherein an elemental width of each of the second plurality of data elements is equal to twice the elemental width of each of the first plurality of data elements.

26. (currently amended) The computer-readable storage medium of claim 14 wherein an elemental width of each of the second plurality of data elements is equal to half the elemental width of each of the first plurality of data elements.

27 - 39. (cancelled)

40. (previously presented) A data processing system comprising:

a bus coupling components in the data processing system;

an external memory coupled to the bus;

a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register.

41. (previously presented) The data processing system set forth in claim 40 wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data.

42. (previously presented) The data processing system set forth in claim 41 wherein the operand register is a 128-bit register and the destination register is a 128-bit register.

43. (previously presented) The data processing system set forth in claim 40 wherein the shift amount is contained in an immediate field of the instruction.

44. (previously presented) The data processing system set forth in claim 40 wherein the shift amount is contained in a register specified by the instruction.

45. (previously presented) A data processing system comprising:

a bus coupling components in the data processing system;

an external memory coupled to the bus;

a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand- register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register.

46. (previously presented) The data processing system set forth in claim 45 wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data.

47. (previously presented) The data processing system set forth in claim 46 wherein the operand register is a 128-bit register and the destination register is a 128-bit register.

48. (previously presented) The data processing system set forth in claim 45 wherein the shift amount is contained in an immediate field of the instruction.

49. (previously presented) The data processing system set forth in claim 45 wherein the shin amount is contained in a register specified by the instruction.

50. (previously presented) A data processing system comprising: (a) a bus coupling components in the data processing system;

an external memory coupled to the bus;

a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination resister, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register.

51. (previously presented) The data processing system set forth in claim 50 wherein the execution unit is operable to execute group shift left instructions on 16• bit, 32-bit and 64-bit signed integer data.

52. (previously presented) The data processing system set forth in claim 51 wherein the operand register is a 128-bit register and the destination register is a 128-bit register.

53. (previously presented) The data processing system set forth in claim 50 wherein the shift amount is contained in an immediate field of the instruction.

54. (previously presented) The data processing system set forth in claim 50 wherein the shift amount is contained in a register specified by the instruction.

55. (currently amended) A computer-readable storage medium: having instructions that cause a computer system to perform operations, the instructions including a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift right instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a sub field of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register.

56. (currently amended) The computer-readable storage medium set forth in claim 55 wherein the computer system is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data.

57. (currently amended) The computer-readable storage medium set forth in claim 56 wherein the operand register is a 128-bit register and the destination register is a 128-bit register.

58. (currently amended) The computer-readable storage medium set forth in claim 55 wherein the shift amount is contained in an immediate field of the instruction.

59. (currently amended) The computer-readable storage medium set forth in claim 55 wherein the shift amount is contained in a register specified by the instruction.

60. (currently amended) A computer-readable storage medium: having instructions that cause a computer system to perform operations, the instructions including a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift right instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register.

61. (currently amended) The computer-readable storage medium set forth in claim 60 wherein the computer system is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data.

62. (currently amended) The computer-readable storage medium set forth in claim 61 wherein the operand register is a 128-bit register and the destination register is a 128-bit register.

63. (currently amended) The computer-readable storage medium set forth in claim 60 wherein the shift amount is contained in an immediate field of the instruction.

64. (currently amended) The computer-readable storage medium set forth in claim 60 wherein the shift amount is contained in a register specified by the instruction.

65. (currently amended) A computer-readable storage medium: having instructions that cause a computer system to perform operations, the instructions including a single group shift left instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift left instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register.

66. (currently amended) The computer-readable storage medium set forth in claim 65 wherein the computer system is operable to execute group shift left instructions on 16-bit, 32-bit and 64-bit signed integer data.

67. (currently amended) The computer-readable storage medium set forth in claim 66 wherein the operand register is a 128-bit register and the destination register is a 128-bit register.

68. (currently amended) The computer-readable storage medium set forth in claim 65 wherein the shift amount is contained in an immediate field of the instruction.

69. (currently amended) The computer-readable storage medium set forth in claim 65 wherein the shift amount is contained in a register specified by the instruction.

70-84. (cancelled)